







Projekts tiek īstenots sadarbībā ar

Development of data compression block, using Huffman coding

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Introduction

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Lossless data compression methods

Entropy type:

- Arithmetic;
- Huffman;
- Golomb;
- Range;
- Shannon-Fano;
- Fibonacci;
- etc.

Dictionary type:

- DEFLATE;
- Lempel-Ziv;
- Run-lenght encoding;
- etc.

Other types:

- Delta;
- Burrows–Wheeler;
- etc.

Huffman coding

Huffman coding is lossless entropy compression algorithm;

Based on variable-length code table called Huffman tree;

Coding process can be divided in two parts:

- creation of Huffman tree;
- creation of code for each symbol in alphabet;

Universal data compression block (UDCB) is based on a particular type of Huffman coding called Canonical Huffman coding.



Canonical Huffman coding

Canonical Huffman coding allows to describe Huffman tree;

Description table is created using one formula and simple «for» loop:

for
$$f \coloneqq 5 \text{ downto } 1 \text{ do } first[f] \coloneqq$$

$$\coloneqq [(first[f+1] + probability[f+1]/2)]$$

where $first[6] \coloneqq 0$

Nr	Huffman codo	Canonical	Nr	Huffman codo	Canonical
M .		Huffman code	111.		Huffman code
1	000	011	9	10100	01000
2	001	100	10	101010	000000
3	010	101	11	101011	000001
4	011	110	12	101100	000010
5	10000	00100	13	101101	000011
6	10001	00101	14	101110	000100
7	10010	00110	15	101111	000101
8	10011	00111	16	110000	000110

Code length	1	2	3	4	5	6
Code "probability"	0	0	4	0	5	7
First number	2	4	3	5	4	0

Development methods

Possible UDCB development methods:

- ASIC (Application-specific integrated circuit) or similar;
- Microcontrollers (Modified C or other languages);
- FPGA (VHDL, LabVIEW environment).

LabVIEW FPGA

LabVIEW* is a system-design platform and development environment;

LabVIEW FPGA is an extension module for LabVIEW to target FPGAs on NI** reconfigurable I/O (RIO) hardware

Implements true parallelism for parallel data processing on FPGA chip in real-time

*Laboratory Virtual Instrument Engineering Workbench **National Instruments



FPGA target device

Xilinx Spartan-3E FPGA Family chip:

- System gates 500K;
- Equivalent Logic Cells 10 476;
- Distributed RAM bits 73K;
- Block RAM bits 360K;
- Dedicated multipliers 20;
- User I/O 232;



ACKNOWLEDGEMENTS

The goal of development is a true parallelism for high speed compression of large amount of data;

Possible to change the capacity of the buffer memory;

UDCB can compress 8 bit input data;

Despite of Huffman coding sequential nature, it is possible to do parallel data processing:

- Data reading;
- Compression of data;
- Data sending.

Structure of UDCB is divided in units which can be implemented in many ways (add new, edit existing)





ACKNOWLEDGEMENTS





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Testbench

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Testing results



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Performance results

Testing for each case – 500 runs:

Symbol	Average clock	Average				
count	counts	time, ms				
3	66809	1,34				
28	141479	2,83				
33	146498	2,93				
168	238394	4,77				
2	60354	1,21				
1	33422	0,67				
256	268958	5,38				



Conclusions and suggestions

UDCB is developed successfully and it is compressing data correctly;

UDCB can be implemented in low power FPGA in data storing subsystem on nano-satellite CubeSAT type satellite;

Implement another Huffman coding type algorithms better performance comparing;

Implementation in other FPGA targets for more accurate and close to real-time testing;

Create adaptive table sending algorithm:

- Unique symbol count <86 then send only coded symbols and their code length;
- Unique symbol count \geq 86 then send whole table but only each symbol code length;

Upgrade UDCB to compress another length data (ex. 16 or 32 bit data);

Upgrade UDCB buffer memory for larger amount of compressible data (ex. 1024 or 2048 symbols).



EIROPAS SAVIENĪBA





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"The laws of probability, so true in general, so fallacious in particular."

- Edward Gibbon