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Projekts tiek īstenots sadarbībā ar LIAA Latvijas Investīciju un attīstības aģentūra Investment and Development Agency of Latvia

Concept of the reconfigurable communication subsystem for custom modulation technique experiments with CubeSats

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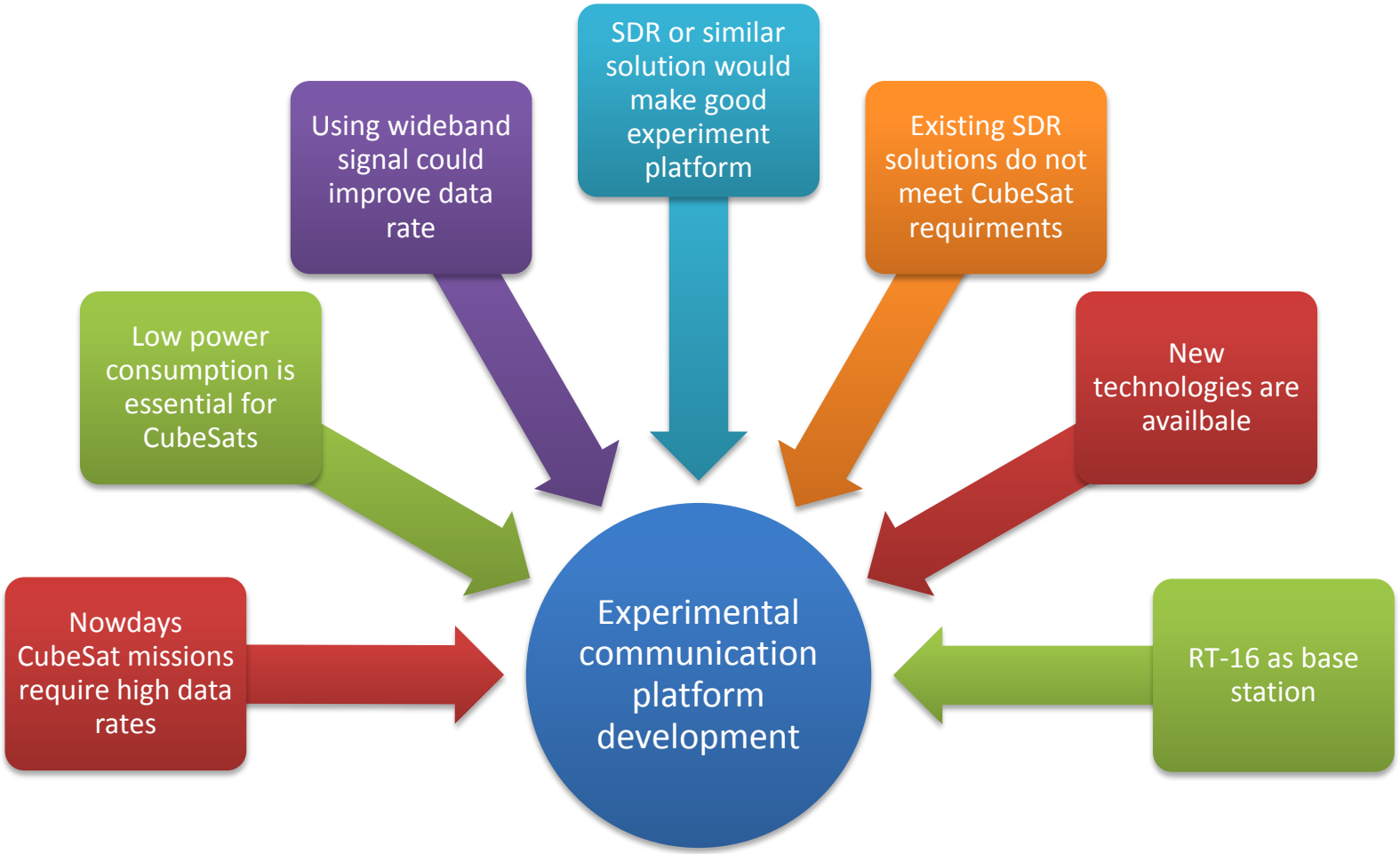
Experimental communication platform



RT-16 link budget advantage

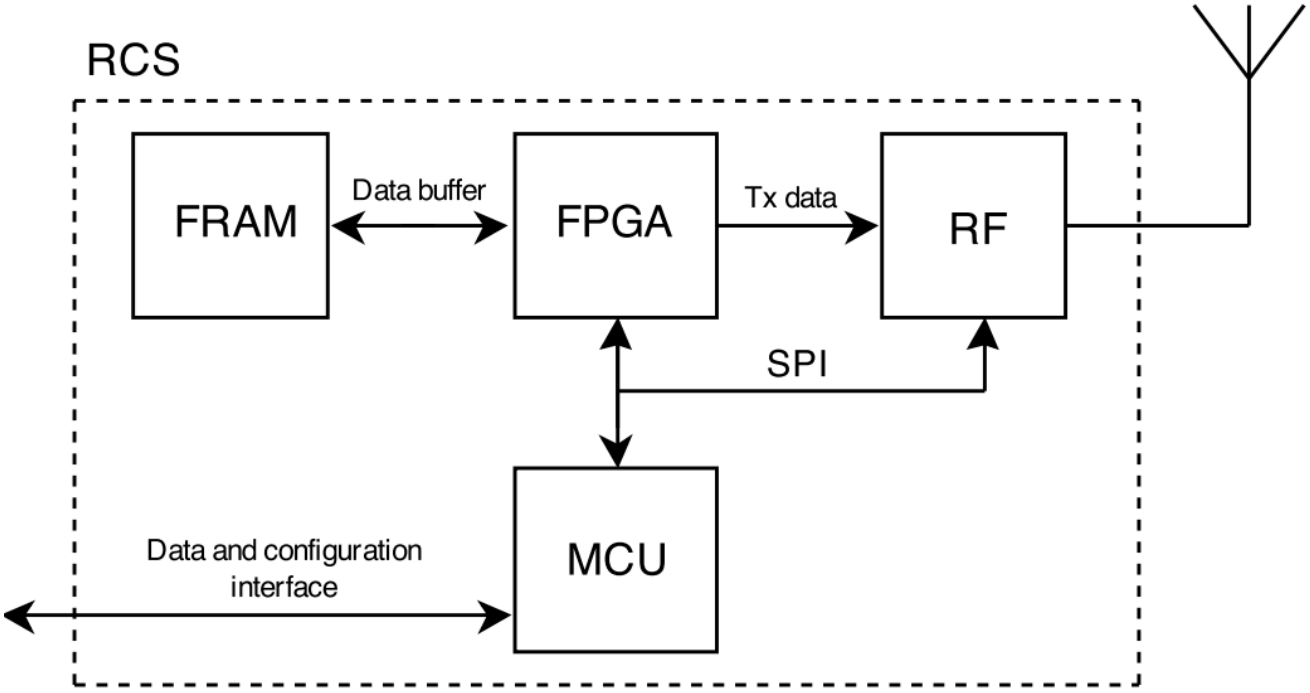
Example:

- DQPSK 2.4 GHz
- 0.5W RF power
- Using simple “warm” receiver
- Data rate 5 Mbps

RF section considerations

- SDR device
- Custom made RF frontend
- Solution from existing communication standards (Wi-Fi, Wi-Max)
- **Relativly new technology - Field Programmable Radio frequency (FPRF) chip**

Reconfigurable Communication Subsystem (RCS)



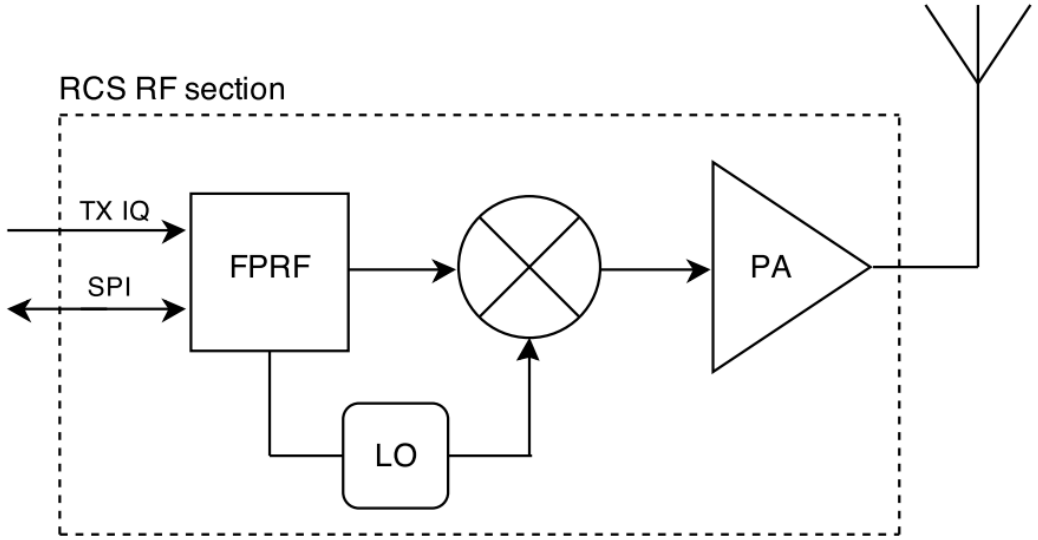
- C-band or S-band downlink
- Estimated data rate up to 10 Mbps
- RF output power 0.5 – 1 W
- Maximum power consumption ~10W
- Reconfigurable frequency, power, modulation, coding etc.

RCS main sections

RF	FPGA	MCU
• Data conversion • Upconversion • Amplification	• High performance digital signal processing • Memory	• Subsystem management • Data interface

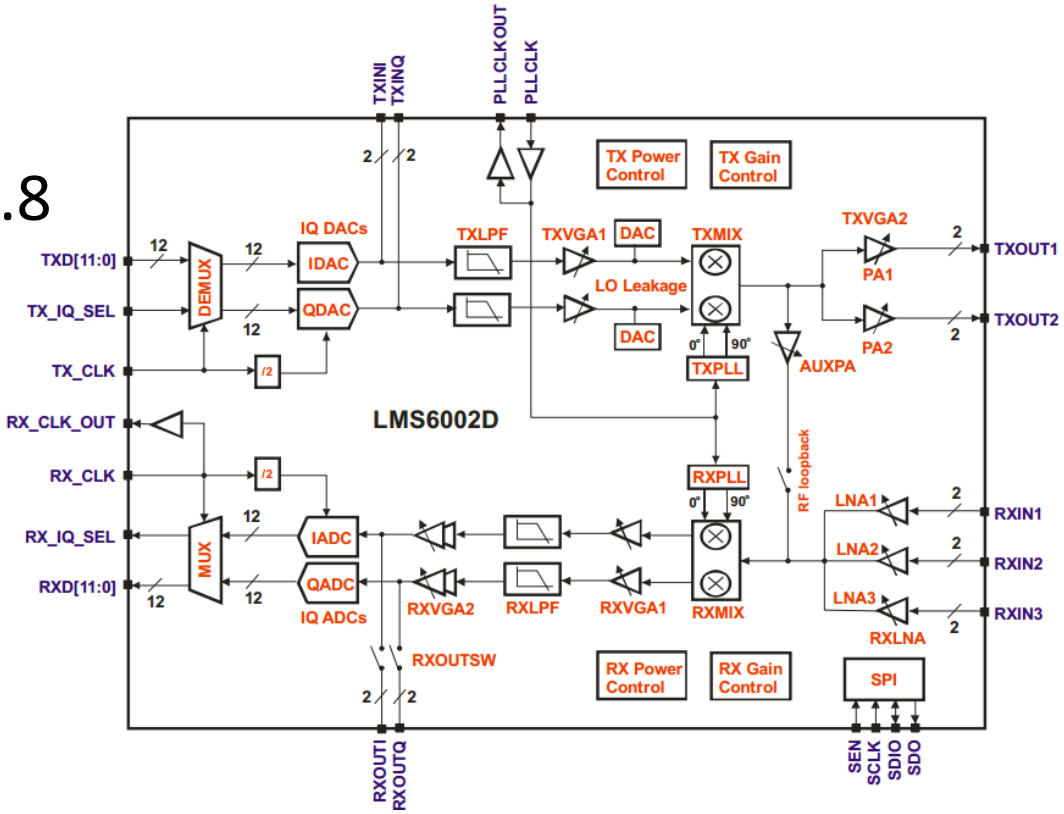
RCS in conjuction with RT-16

- Requires frequency to be up-converted form 3.8 to 5.8 GHz
- Up-conversion significantly reduces power and PCB area budget
- S-band can be used (RT-16 would need a new receiver)



FPRF

- Single chip transceiver
- Integrated ADCs/DACs
- Operating from 0.3 to 3.8 GHz
- Higly reconfigurable architecture
- Requires less PCB area and power



MCU: programm memory

MCU is the hart of the system - reliability in free space flight

	Flash	EEPROM	SRAM	FRAM
Non-volatile	Yes	Yes	No	Yes
Write endurance	10 000	~500 000	Unlimited	1 million billion (i.e. 10^{15})
Write speed (for 13 kB)	1s	2s	<10ms	10ms
Average active power (µA/MHz)	260	Up to 10 mA	<60	80
Dynamics bit addressable programmability	No	No	Yes	Yes

MCU selection

Part Number	GPIO	Package Group	Estimated Package Size (WxL)(mm^2)
MSP430FR5849	33	TSSOP, VQFN	40VQFN: 6 x 6: 36 mm2, 38TSSOP: 6.2 x 12.5: 103 mm2
MSP430FR5859	33	TSSOP, VQFN	40VQFN: 6 x 6: 36 mm2, 38TSSOP: 6.2 x 12.5: 103 mm2
MSP430FR5869	40	VQFN	48VQFN: 7 x 7: 49 mm2
MSP430FR5949	33	TSSOP, VQFN	40VQFN: 6 x 6: 36 mm2, 38TSSOP: 6.2 x 12.5: 103 mm2
MSP430FR5959	33	TSSOP, VQFN	40VQFN: 6 x 6: 36 mm2, 38TSSOP: 6.2 x 12.5: 103 mm2
MSP430FR5969	40	VQFN	48VQFN: 7 x 7: 49 mm2
MSP430FR59691	40	VQFN	48VQFN: 7 x 7: 49 mm2

- FRAM non-volatile memory (64 KB FRAM and 2 KB SRAM)
- Ultra-low-power 16-bit MSP430 CPU

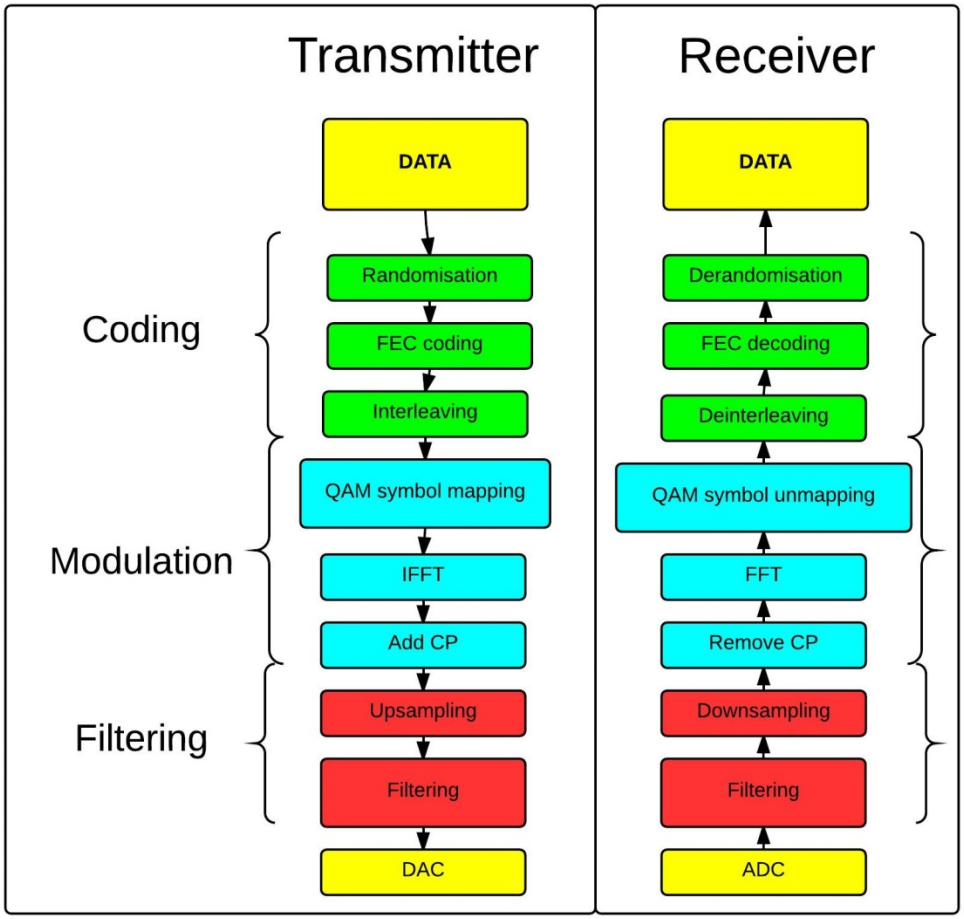
Command groups

- FPGA- program, reconfigure, upload, memory, debug
- FPRF- reconfiguration
- General- RCS status and control

Why FPGA?

Video

FPGA based pipelined signal-path



Functionality:

- Coding/decoding
- Modulation/demodulation
- Upsampling/downsampling and filtering.
- All operations must be performed simultaneously in pipeline.

The bottleneck – high troughput IFFT/FFT core.

Requirements:

- Low power consumption
- High throughput FFT/IFFT core
- Sufficient amount of DSP blocks

Microsemi IGLOO2 Family

Advantages:

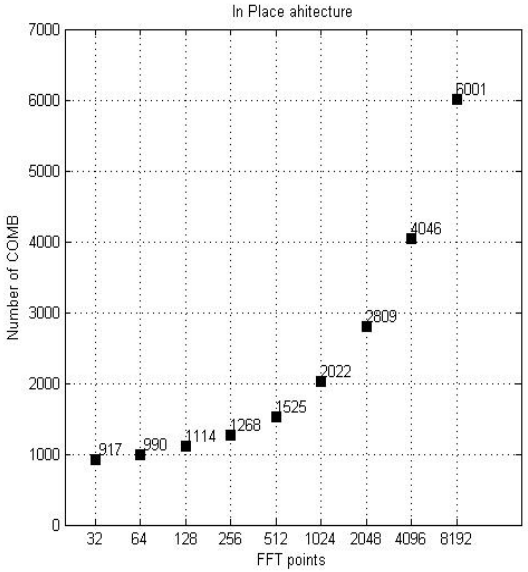
- Flash based FPGA technology
- Very low power consumption
- Flash*Freeze mode

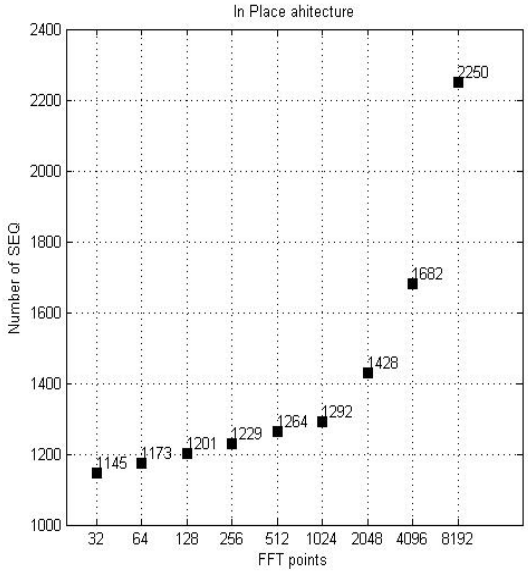
IGLOO2 Delivers Up To

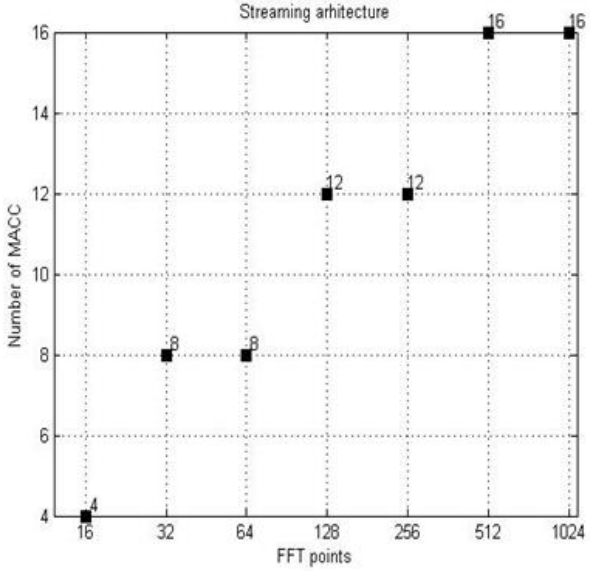
- ***3X Lower Static Power***
- ***25% Lower Total Power***

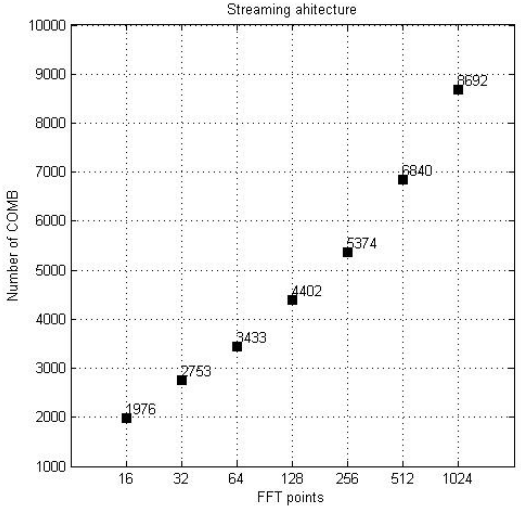
Overview of IGLOO2 family

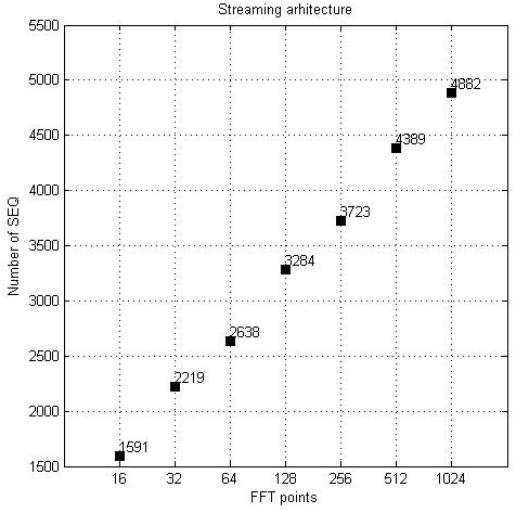
	M2GL005	M2GL010	M2GL025	M2GL050	M2GL090	M2GL100	M2GL150
Maximum Logic Elements (4LUT + DFF)*	6,060	12,084	27,696	56,340	86,316	99,512	146,124
Math Blocks (18x18)	11	22	34	72	84	160	240
Total RAM (K bits)	703	912	1104	1826	2586	3552	5000


In Place ahitecture
Number of COMB
FFT points
917
990
1114
1268
1525
2022
2809
4046
6001


In Place ahitecture
Number of SEQ
FFT points
1145
1173
1201
1229
1264
1292
1428
1682
2250


Streaming arhitecture
Number of MACC
FFT points
4
8
8
12
12
16
16


Streaming ahitecture
Number of COMB
FFT points
1976
2753
3433
4402
5374
6840
8692


Streaming arhitecture
Number of SEQ
FFT points
1591
2219
2638
3284
3723
4389
4882

FPGA data storage

- Data buffer to ensure high data rate transmission;
- FPGA (M2GL010) memory resources:
  - 256 kB Embedded Nonvolatile Memory;
  - 64 kB Emebedded SRAM;
  - 400 kb FPGA fabric memory;
- Trade-off between technology of external RAM:
  - FRAM: less memory, lower power consumption;
  - MRAM: more memory, higher power consumption during write cycle.

Future work

- Transmitter > transceiver
- Up-converter design
  - low power consumption
  - low distortions
- Power amplifier design
  - efficient to reduce power consumption
  - linear enough
- FRAM/MRAM?
- new tech MCUs / FPGA based MCU?
- watch for a new generation FPRFs

Conclusion

- Four main components board design is proposed:
  - MCU: MSP430FR5869
  - FPGA: Microsemi IGLOO2 M2GL010
  - FPRF: LM6002D
  - FRAM/MRAM
- Manufacturers provide information about their products in they own way
- Only downlink functionality will be implemented in initial design
- S-band will be used for initial design, upgrade to C in later versions (experiments with up-converter solutions)
- Development is on the way to make prototype

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Thank You!

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